Mohammad Saeed Rajabi

Hardware Architect Embedded Systems R&D Expert

Personal Information

- **Age:** 26
- Gender: Male
- **Location:** Semnan, Semnan Province
- Marital Status: Single
- **Military Service:** Educational Exemption

Contact Information

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- **Current Residence:** Vali-e-Asr Intersection, Tehran

Education

- Master's Degree
  - **Major:** Computer Systems Architecture
  - **University:** Amirkabir University of Technology (Tehran Polytechnic)
  - **GPA:** 18.50
- Bachelor's Degree
  - **Major:** Computer Engineering
  - **University:** Semnan University (State)
  - **GPA:** 16.79

Summary

Hardware Architect and Embedded Systems Research and Development Expert with over 4 years of professional experience. Holds a Master's degree in Computer Systems Architecture from Amirkabir University of Technology. Focused on cutting-edge research in computer architecture and novel memory technologies, alongside extensive industrial experience in designing control modules, developing embedded operating systems, and implementing Internet of Things (IoT) infrastructures.

Research Interests

- **Advanced Computer Architecture and novel memory technologies, with a focus on magnetic memories (Multi-Retention Level MRAM).**
- **Cache Optimization and data migration strategies.**
- **Full-System Simulation and the evaluation of processing architectures.**
- **Industrial-scale Internet of Things (IoT) and real-time embedded systems design.**

Work Experience & Notable Industrial Projects

- **Mobin Saman Company | Embedded Systems R&D Expert**
  - **Designed and developed industrial testing equipment for automotive production lines, including end-of-line vehicle testers, custom wiring harness testers, and seat heater/actuator testers.**
- **Amirkabir University of Technology | FPGA Specialized Course Instructor**
  - **Instructed the undergraduate Computer Architecture Laboratory under the supervision of Dr. Hamidreza Zarandi.**
- **National Iranian Tanker Company (NITC) | Ship Data Aggregation and Management Project**
  - **Designed and developed a centralized platform for the collection, integration, and normalization of operational data from sensors and control modules, featuring highly stable data transmission mechanisms.**
- **Freelance and Infrastructure Projects**
  - **Implemented monitoring systems using the MQTT protocol and designed hardware utilizing ARM, AVR, and ESP microcontrollers.**

About Me

I consider myself a responsible individual regarding my duties in both professional and social environments. When facing issues and challenges, I always strive to respond in a flexible and efficient manner.

Foreign Languages

- English: Intermediate

Training Courses

- Comprehensive C++ Programming (30 hours)
- ST Microcontroller Development (30 hours)
- VHDL Hardware Description Language (30 hours)
- Printed Circuit Board (PCB) Design (30 hours)

- Executed advanced network configurations and virtualization using Proxmox and MikroTik routers.

Academic & Research Projects

- Accurate structural evaluation and cycle-accurate execution in the gem5 simulator under Full-System mode.
- Transistor-level design and implementation of a 4-Megabit Random Access Memory (RAM) using HSPICE.
- Software development and CAN protocol implementation on STM32 microcontrollers, including the creation of a Software Bootloader.
- Customization and compilation of a Custom Ubuntu operating system for Raspberry Pi boards.
- Conceptual design and implementation of a smart glove capable of converting sign language to speech.
- Implementation of Big Data projects by setting up HDFS within the Hadoop and YARN ecosystems.

Technical & Engineering Skills

- Programming & Hardware Description Languages: Advanced proficiency in C/C++; intermediate skills in Python, Assembly, VHDL, HTML, and CSS.
- Hardware Design & Architecture: Expertise in the ARM Cortex family and embedded controllers such as NXP i.MX6, Raspberry Pi, STM32, ESP, and FPGA development. Advanced PCB design using Altium Designer; intermediate proficiency in HSPICE, Vivado/ISE, and STM32CubeIDE.
- Embedded Systems Development: Hardware and software development based on STM32 and NXP, UI development with Qt, and Custom Kernel Build. Implementation of industrial communication protocols including SPI, CAN/FDCAN, UART, and Socket programming.
- Embedded Operating Systems (OS): Building and customizing distributions using Buildroot and the Yocto Project.
- Infrastructure & Tools: Intermediate skills in Linux, system management, containerization with Docker and Proxmox, Git version control, and SQLite databases.

Publications & Academic Papers

- Title: Beyond One-Hot: CatBoost for Heating and Cooling Load Prediction
- Authors: Shayan Naghizadeh, Mohammad Saeed Rajabi (Second Author), Ehsan Nazarfard

- **Conference: 16th International Conference on Information and Knowledge Technology (IKT), 2025**
- **Affiliation: Department of Computer Engineering, Amirkabir University of Technology**
- **Research Achievements:**
  - **Developed and evaluated advanced machine learning models using the ENB2012 dataset to accurately predict heating and cooling loads of buildings, aiming to improve energy efficiency.**
  - **Applied the novel CatBoost gradient boosting algorithm, which natively supports categorical variables, successfully overcoming the complexities of conventional preprocessing methods like One-Hot Encoding.**
  - **Achieved the lowest prediction error among all evaluated models, registering up to a 30% reduction in MAE and RMSE metrics compared to powerful algorithms such as XGBoost and Random Forest Regression.**
  - **Maintained exceptionally high prediction accuracy, recording a coefficient of determination (R^2) greater than 0.990 for both heating and cooling loads.**
  - **Feature-Importance analysis revealed that physical factors such as compactness, overall height, and surface area possess the highest predictive impact, aligning perfectly with the physical principles of heat transfer.**

Comprehensive Master's Thesis Research Project

- **Thesis Title: Energy-Aware Memory Management for IoT Devices based on Multi-Retention MRAM**
- **University: Amirkabir University of Technology (Tehran Polytechnic) - Department of Computer Engineering**
- **Supervisor: Dr. Hamed Farbeh**
- **Focus Area: Spintronics Microarchitecture, Reliability of Embedded Systems, and Internet of Things (IoT)**

- **Problem Statement & Research Gap: Edge processing nodes spend extended periods in the Standby phase, resulting in severe leakage power dissipation in volatile memories (SRAM). While replacing these with non-volatile magnetic memory (STT-MRAM) eliminates static power, insisting on long-term (10-year) data retention imposes severe write energy and latency penalties on the system. Previous research has typically struggled with this challenge by relying on rigid circuit modifications or by ignoring the correlated error triangle (retention, read disturbance, and early write).**

- **Proposed Architecture & Innovations: This thesis presents an interdisciplinary solution across two layers – device physics and system microarchitecture – to drastically reduce energy consumption:**
  - **Retention Relaxation: Intentional reduction of the thermal stability factor (Δ) at the PMTJ cell physical layer to exponentially decrease the critical switching current (I_{c0}).**
  - **Heterogeneous Cache: Allocating memory arrays into high-retention zones (10-year) for persistent data and ultra-low retention zones (microsecond/millisecond scale) for transient data, which drops write energy down to the 200 femtojoule (fJ) threshold.**
  - **Static-Circuit Dynamic Routing Strategy: Intelligent and dynamic routing of data blocks to corresponding memory zones based on traffic patterns, bypassing the need for complex current pulse width manipulations at the circuit layer.**
  - **Reliability Monitor: Proposing a model to contain the hardware error triangle and prevent the corruption of sensitive data prior to a refetch operation.**

- **Modeling & Simulation Infrastructure (Methodology & Tools): To validate the efficiency of this architecture, a Dual-Stack Evaluation framework was developed:**
  - **gem5 System-Level Simulator: Configuration and execution of cycle-accurate simulations under Full-System mode to extract memory traces, hit/miss rates, and to evaluate pipeline stall timings.**
  - **NVSim Circuit and Physical Modeler: Calibration of fine-grained solid-state physics parameters (e.g., TMR ratio and free layer dimensions) to precisely extract applied current, dynamic read/write energy, leakage power, and on-chip area footprint.**
  - **Integrated Analyzer: Synthesizing gem5 traffic outputs with NVSim energy models to generate the final power and performance profile of the proposed microarchitecture.**

- **Key Research Achievements:**
  - **Established a reasoned mathematical connection between the quantum physics of magnetic switching and cache management algorithms.**
  - **Significantly reduced Dynamic Write Energy in cache memories, achieving parity with volatile memories.**
  - **Enhanced the lifecycle and the Power-Performance Trade-off in edge processing nodes.**